



Application Note

AN_299

FT800_FT801_Internal_Clock _Trimming

Version 1.0

Issue Date: 2014-03-04

The FTDI FT800 and FT801 video controllers offer a low cost solution for embedded graphics requirements. In addition to the graphics, touch screen inputs and an audio output provide a complete human machine interface to the outside world.

This application note will provide a programming sequence on how to trim the chip's internal clock for higher accuracy so that applications may run without an external crystal.

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1 Introduction

The FT800/FT801 operates as an SPI or I²C peripheral to a main system processor thus providing a low-cost, yet complete, human interface experience by the incorporation of graphics rendering, touch screen sensing and audio capabilities. It is controlled over a low-bandwidth SPI or I²C interface allowing practically any microcontroller to be used.

The FT800/FT801 supports both internal clock and external clock operations. The internal clock is a relaxation oscillator which can be trimmed by a register for higher accuracy, so that for many applications external crystal or clock is not required.

**DISPLAY****AUDIO****TOUCH**

2 Clock Circuit

The FT800/FT801 clock circuits include input clock source and PLL. Clock source can be selected between internal relaxation oscillator and 12MHz crystal oscillator. The PLL will multiply the input clock by 4(default) to generate nominal 48MHz system clock, which supply the clock for all internal registers, memories and processors.

The internal relaxation oscillator clock ranges from 4.46MHz to 12.11MHz (untrimmed) and can be trimmed by writing to the trim register (REG_TRIM). After trimming the clock can reach 12MHz at the tuning accuracy of +/-2.5%. The tuned frequency may vary within +/-3% across operating temperature and voltages.

The FT800/FT801 has 2 output pins which can be used to monitor and calculate the system clock frequency. The PCLK out pin will output a clock with its frequency equals to f_{sys_clk} / REG_PCLK (REG_PCLK programmed to none-zero value). For example, assume the REG_PCLK is programmed to 5, and the PCLK output frequency is measured at 9.6MHz, in this case the $f_{clk_sys} = 5 * 9.6MHz = 48MHz$.

Alternatively, f_{clk_sys} can be calculated by measuring the clock frequency on AUDIO_L pin. The AUDIO_L pin outputs PWM signal for mono audio signal. The frequency of the PWM signal is $f_{clk_sys} / 512$. If the measured frequency on AUDIO_L pin is 93.75kHz, then $f_{clk_sys} = 512 * 93.75kHz = 48MHz$.

The FT800/FT801 clock circuit is shown in Figure 2-1. For applications using the internal relaxation clock only, the external crystal is not required. In this case the X1/CLKIN pin shall be tied to GND and the X2 pin shall be left unconnected, as shown in Figure 2-2.

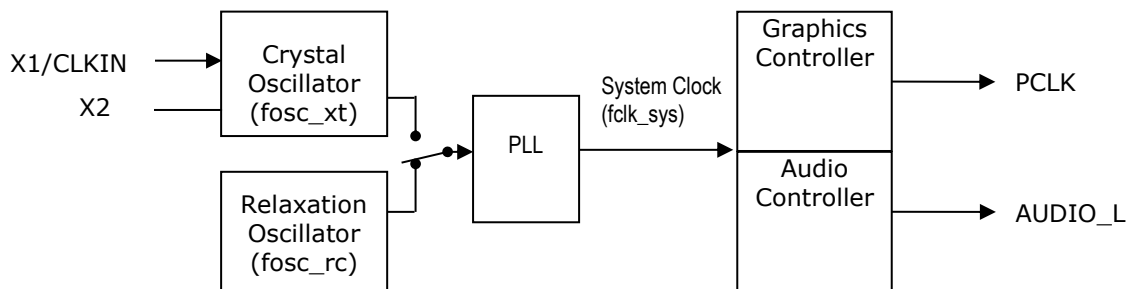


Figure 2-1 FT800/FT801 clock circuit

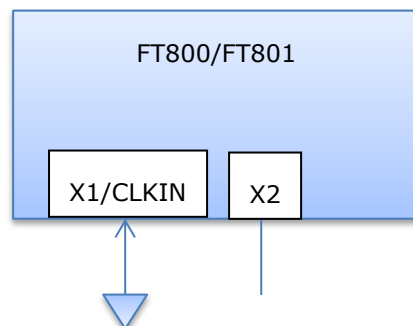


Figure 2-2 internal clock mode pin connection

3 Clock Trimming Sequence

The internal relaxation oscillator frequency is determined by the RC value of the oscillator circuit. The on-chip resistor and capacitor have quite a wide variance across the wafer process. By tuning the effective RC value through registers, it is possible to trim the clock frequency for higher accuracy.

3.1 Useful Register Description

There are a number of registers involved in the clock trimming sequences. This section describes in detail the function of these registers.

REG_TRIM

The trim register REG_TRIM has 5 valid bits Trim[4:0], which allows total 32 trim settings. Default is 0. When increasing the trim register value the effective RC value of the oscillator decrease, so that the clock frequency increases accordingly.

REG_CLOCK

This 32-bit register counts the number of FT800/FT801 main clock cycles since reset. By reading this register, the host MCU can calculate the main clock frequency based on the accurate timer in the MCU.

REG_FREQUENCY

This 32-bit register stores the value of the current main clock frequency. Software needs to update this register once the clock trimming is completed.

3.2 Trimming Method

During power on initialization, software can trim the internal relaxation oscillator clock to the desired value. The target value is 12MHz, so that the main clock will operate at 48MHz.

After the chip is put into the active mode, the internal clock, PLL, will be running and the system main clock will be available. The REG_CLOCK will start to count every main clock cycle. By reading the REG_CLOCK twice in a defined interval (ie. 1us based on MCU clock or timer), the main clock frequency can be calculated. If the measured frequency is lower than the target, increase the value of REG_TRIM. Repeat this operation until the measured frequency is within +/-3% of the target frequency.

3.3 Detailed Sequences

The following steps provide a detailed programming sequence to trim the internal clock.

1. After a hardware reset (power on or toggling PD_N pin), the FT800/FT801 enters STANDBY mode. The internal relaxation oscillator clock is selected as the clock source of the PLL. Both the internal clock and the PLL are turned on, but the main clock to the core logic is turned off.
2. Set the chip to ACTIVE mode by doing a dummy read operation through host interface (SPI or I2C).
3. Measure the current clock frequency
 - a. Read REG_CLOCK as t0
 - b. Delay 1us
 - c. Read REG_CLOCK as t1
 - d. Calculate the clock frequency $f = (t1-t0) / 1\mu s$
4. If the measured frequency f is less than 48MHz - 3%, increase the REG_TRIM register by 1
5. Repeat steps 3 and 4 until the measured frequency is within 48MHz +/- 3%, or the REG_TRIM already reaches the maximum value of 31 (which is unlikely since the trimming range is defined to be able to tune the clock to the target)

6. Write the final measured frequency f to REG_FREQUENCY

Below is the sample C code for internal clock trimming, used by the Gameduino 2 application:

```
/******  
  
#define REG_CLOCK    0x102408  
  
uint32_t GDClass::measure_freq(void)  
{  
    unsigned long t0 = GDTR.rd32(REG_CLOCK);  
    delayMicroseconds(15625);  
    unsigned long t1 = GDTR.rd32(REG_CLOCK);  
    return (t1 - t0) << 6;  
}  
  
#define REG_TRIM      0x10256C  
#define REG_FREQUENCY  0x10240C  
#define LOW_FREQ_BOUND 4704000UL  
  
void GDClass::tune(void)  
{  
    unsigned char i = 0;  
    uint32_t f;  
    for (byte i = 0; (i < 31) && ((f = measure_freq()) < LOW_FREQ_BOUND); i++)  
        GDTR.wr(REG_TRIM, i);  
    GDTR.wr32(REG_FREQUENCY, f);  
}
```

Since the REG_TRIM will reset to 0 every time a hardware reset happens, it is required to perform the clock trimming sequence in the reset initialization routine.

4 Contact Information

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Appendix A – References

Document References

[EVE Product Page](#)

[FT800 Datasheet](#)

[FT801 Datasheet](#)

[FT800 Programmers Guide](#)

[VM800C Datasheet – Credit Card sized development board with FT800](#)

[VM800B Datasheet – Bezel-mounted Display with FT800](#)

[AN_240 EVE From the Ground Up](#)

[AN_259 FT800 Example with 8-bit MCU](#)

Acronyms and Abbreviations

Terms	Description
GND	Ground
EVE	Embedded Video Engine
I ² C	Inter-Integrated Circuit
PLL	Phase Lock Loop
SPI	Serial Peripheral Interface

Appendix B – List of Tables & Figures

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Appendix C – Revision History

Document Title: AN_299 FT800_FT801_Internal_Clock_Trimming
Document Reference No.: FT_000987
Clearance No.: FTDI# 373
Product Page: <http://www.ftdichip.com/EVE.htm>
Document Feedback: [Send Feedback](#)

Revision	Changes	Date
1.0	Initial Release	2014.03.04