TN_120 FT232R Errata Technical Note

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The intention of this errata technical note is to give a detailed description of any known functional or electrical issues with the FTDI FT232R devices.
The current revision of the FT232R is **revision B, released May 2007.** At the time of releasing this Technical Note there are no known issues with this silicon revision.

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1 FT232R Revision

FT232R part numbers are listed in **Table 1.** The letter at the end of date code identifies the device revision.

The current revision of the FT232R is **revision B, released May 2007.** At the time of releasing this Technical Note there are no known issues with this silicon revision.

Part Number	Package
FT232RL	28 Pin SSOP
FT232RQ	32 Pin QFN

Table 1 FT232R Part Numbers

This errata technical note covers the revisions of FT232 listed in **Table 2**.

Revision	Notes
A	First device revision
B	Second Device revision

Table 2 FT232R Revisions

2 Errata History Table – Functional Problems

Functional Problem	Short description	Errata occurs in device revision
FT232R	PWREN# signal will not be stable during enumeration – 3 pulses.	A

2.1 Errata History Table – Electrical and Timming Specification Deviations.

Deviations	Short description	Errata occurs in device revision
FT232R	Cannot set VCCIO below 2.6V due to internal RESET# pullup	A

3 Functional Problems of FT232R

3.1 Revision A

3.1.1 PWREN# pulses during enumeration

Introduction:

PWREN# is an output to signal if the device is enumerated and awake (logic 0) or if it is in reset/suspend (logic 1)

Problem:

During enumeration the pins were configured as outputs and as a consequence of the 3 resets required during enumeration the device toggled 3 times giving a false indication that the device was ready to use.

Workaround:

There are no known workarounds available. This issue is corrected at silicon revision B.

Package specific:

The effected packages are listed in **Table 3.**

Package	Applicable (Yes/No)
FT232RL	Y
FT232RQ	Y

Table 3

3.1.2 BitBang Mode variable Pulse Width

Introduction:

BitBang is a mode the device may be put into to allow free running data to be clocked in/out of the device without any control bits.

Problem:

The output may be clocked out at different speeds to allow for different pulse widths. However this clocking stage is not synchronized with the incoming data and can result in the pulse widths varying unexpectedly on the output.

Workaround:

Set the clock divisor to 1 (baud rate = 3,000,000) and pad the data field with extra 1's or 0's to achieve the required pulse width for each bit.

Package specific:

The effected packages are listed in Table 4

Package	Applicable (Yes/No)
FT232RL	Y
FT232RQ	Y

Table 4

3.1 Revision B

There are no known new functional issues specific to revision B.

4 Electrical and Timing specification deviations of FT232R

4.1 Revision A

4.1.1 VCCIO cannot be set below 2.6V

Introduction:

The FT232R device is specified to handle IO down to 1.8V.

Problem:

The FT232R device contains an internal pullup (200k) on RESET#. This is wired to VCCIO and not VCC. If VCCIO is below 2.6V the device will not come out of reset.

Workaround:

There are no known workarounds available. This issue is corrected at silicon revision B.

Package specific:

The effected packages are listed in Table 5.

Package	Applicable (Yes/No)
FT232RL	Y
FT232RQ	Y

Table 5

4.1 Revision B

There are no known functional problems with revision B.

5 FT232R Package Markings

FT232R is available in two RoHS Compliant packages, 32 pin QFN and 28 pin SSOP. An example of the markings on each package is shown in

Figure 5-1..

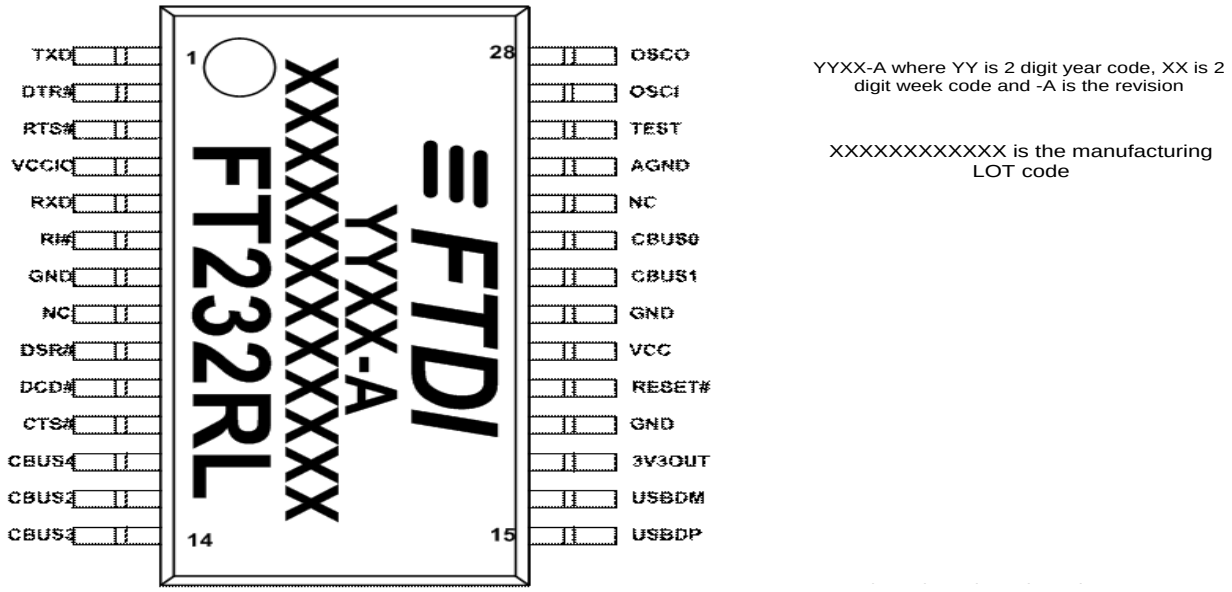

Figure 5-1 Package Markings – 28 SSOP

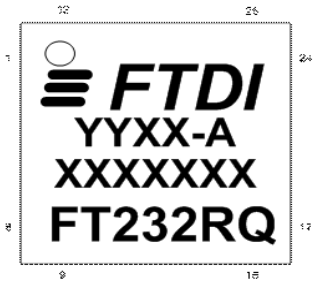

Figure 5-2 Markings – 32 QFN

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Appendix C – Revision History

Version 1.0 First Release 05/11/2010

