



## **TN\_125 FT2232H Errata Technical Note**

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The intention of this errata technical note is to give a detailed description of known functional or electrical issues with the FTDI FT2232H devices.

The current revision of the FT2232H is **revision C, released March 2010.**

**Future Technology Devices International Limited (FTDI)**

Unit1, 2 Seaward Place, Centurion Business Park, Glasgow G41 1HH United Kingdom

Tel.: +44 (0) 141 429 2777 Fax: + 44 (0) 141 429 2758

E-Mail (Support): [support1@ftdichip.com](mailto:support1@ftdichip.com) Web: <http://www.ftdichip.com>

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## 1 FT2232H Revision

FT2232H part numbers are listed in **Table 1**. The letter at the end of date code identifies the device revision.

The current revision of the FT2232H is **revision C, released March 2010**. At the time of releasing this Technical Note there are one known issues with this silicon revision. A workaround is provided for this issue.

Part Number	Package
FT2232HL	64 Pin LQFP
FT2232HQ	64 Pin QFN

**Table 1 FT2232H Part Numbers**

This errata technical note covers the revisions of FT2232H listed in **Table 2**.

Revision	Notes
A	First device revision
B	Second device revision
C	Third device revision

**Table 2 FT2232H Revisions**

## 2 Errata History Table – Functional Problems

Functional Problem	Short description	Errata occurs in device revision
FT2232H	Error reading EEPROM interface	A
FT2232H	Error reading internal FIFO in 245 Synchronous FIFO mode	A
FT2232H	3 Phase clocking in MPSSE mode incorrect	A
FT2232H	Wait on IO1 not functioning in CPU Emulation mode	A, B
FT2232H	Double bytes read in CPU Emulation mode	A, B, C

### 2.1 Errata History Table – Electrical and Timing Specification Deviations.

Deviations	Short description	Errata occurs in device revision
Suspend timer failure (USB Chapter 9 Compliance)	The USB specification requires a maximum time to suspend of 3.125ms. The device takes upto 4ms to suspend.	A, B

### 3 Functional Problems of FT2232H

#### 3.1 Revision A

##### 3.1.1 Error reading EEPROM Interface

**Introduction:**

The FT2232H uses an external EEPROM to store USB descriptors. These descriptors must be correctly read for the device to be properly identified and configured.

**Problem:**

There is an issue that under the right conditions the internal address counter can increment by 2 (incorrectly). This appears as though the data read from the EEPROM has missed a byte.

**Workaround:**

There are no known workarounds available. This issue is corrected at silicon revision B.

**Package specific:**

The effected packages are listed in Table 3.

Package	Applicable (Yes/No)
FT2232HL	Y
FT2232HQ	Y

**Table 3**

##### 3.1.2 Error reading internal FIFO in 245 Synchronous FIFO mode

**Introduction:**

The FT2232H uses an internal FIFO to store received data from the synchronous FIFO interface. This FIFO is addressed one byte at a time.

**Problem:**

There is an issue that under the right conditions the internal address counter can increment by 2 (incorrectly). This appears as though the data read from the FIFO has missed a byte.

**Workaround:**

There are no known workarounds available. This issue is corrected at silicon revision B.

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**Package specific:**

The effected packages are listed in Table 4.

Package	Applicable (Yes/No)
FT2232HL	Y
FT2232HQ	Y

**Table 4**

### 3.1.3 3 Phase clocking in MPSSE mode incorrect

**Introduction:**

The FT2232H introduced a new function to the MPSSE mode called 3 phase clocking to allow data to be clocked on both edges.

**Problem:**

3 Phase clocking was not being enabled.

**Workaround:**

There are no known workarounds available. This issue is corrected at silicon revision B.

**Package specific:**

The effected packages are listed in Table 5.

Package	Applicable (Yes/No)
FT2232HL	Y
FT2232HQ	Y

**Table 5**

## 3.2 Revision B

### 3.2.1 Wait on IO1 not functioning in CPU Emulation mode

**Introduction:**

The FT2232H has a "Wait On IO" feature in CPU mode to allow the processor to stop until the IO pin changes state.

**Problem:**

The Wait on IO is supposed to be routed to IO1. It is not.

**Workaround:**

There are no known workarounds available. This issue is corrected at silicon revision C.

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**Package specific:**

The effected packages are listed in Table 3.

Package	Applicable (Yes/No)
FT2232HL	Y
FT2232HQ	Y

**Table 6**

### 3.3 Revision C

#### 3.3.1 Double bytes read in CPU Emulation mode

**Introduction:**

The FT2232H has a CPU Emulation mode for transferring data.

**Problem:**

When reading a byte of data in CPU emulation mode the data is repeated. That is each byte of data is returned twice.

**Workaround:**

Switch off the divide by 5 clock divisor to resolve this problem (Command \$8A)

**Package specific:**

The effected packages are listed in Table 7.

Package	Applicable (Yes/No)
FT2232HL	Y
FT2232HQ	Y

**Table 7**

## 4 Electrical and Timing specification deviations of FT2232H

### 4.1 Revision A

#### 4.1.1 Suspend Timer Failure

**Introduction:**

The FT2232H has the ability to be put into suspend by the host to conserve power usage.

**Problem:**

The USB specification chapter 9 compliance tests require the device to go into suspend within 3.125ms. The device is taking upto 4ms to enter suspend state.

**Workaround:**

There are no known workarounds available. This issue is corrected at silicon revision C.

**Package specific:**

The effected packages are listed in Table 8.

Package	Applicable (Yes/No)
FT2232HL	Y
FT2232HQ	Y

**Table 8**



## 5 FT2232H Package Markings

FT2232H is available in a RoHS Compliant package, 64 pin LQFP and 64 pin QFN. An example of the markings on the package is shown in Figure 3-1.

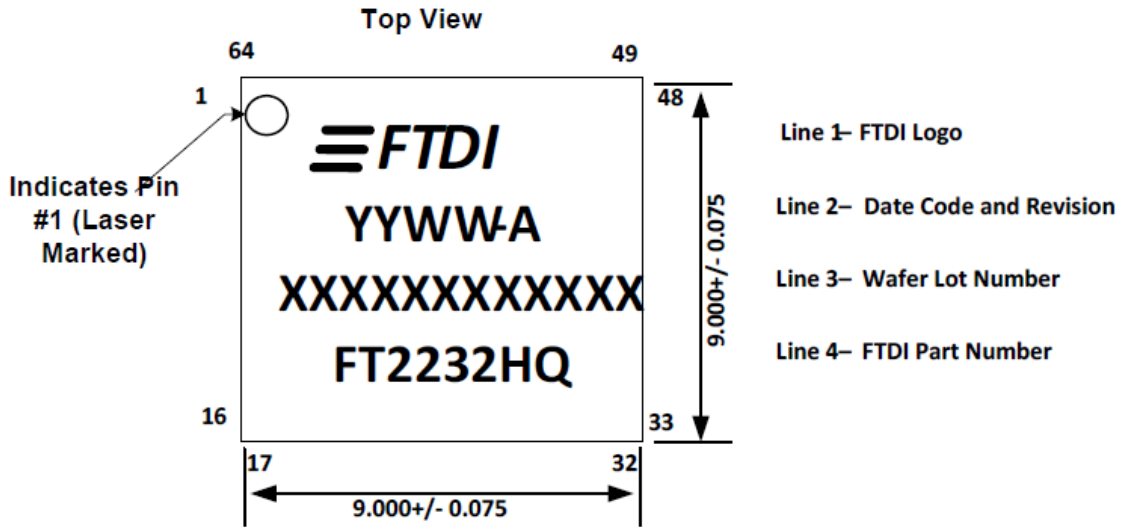


Figure 5-1 Package Markings – FT2232HQ

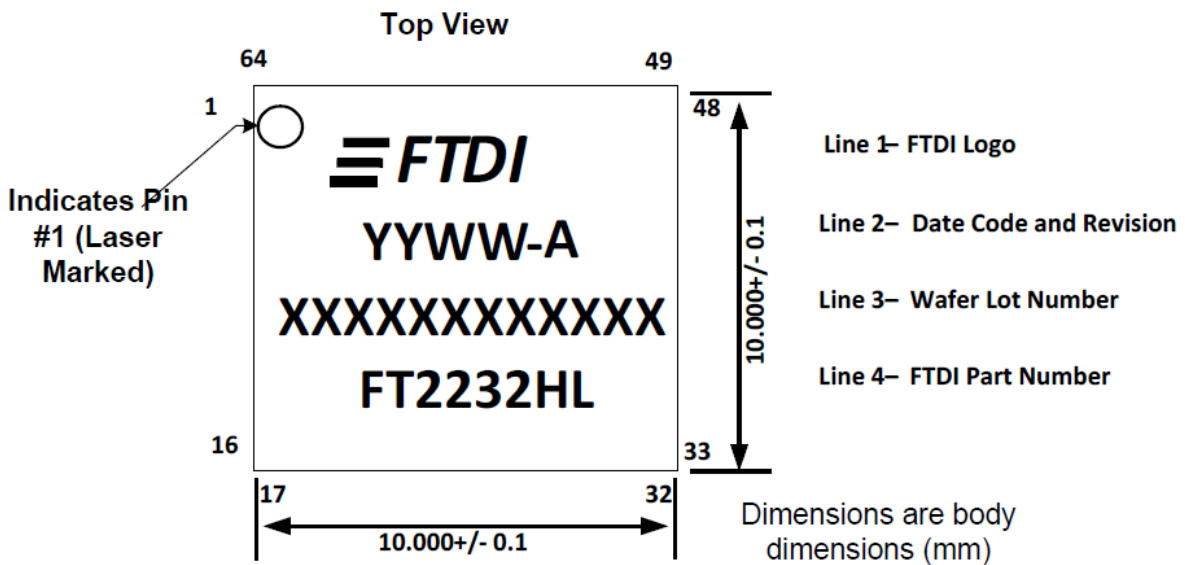


Figure 5-2 Package Markings – FT2232HL

## 6 Contact Information

### Head Office – Glasgow, UK

Future Technology Devices International Limited  
Unit 1, 2 Seaward Place, Centurion Business Park  
Glasgow G41 1HH  
United Kingdom

Tel: +44 (0) 141 429 2777  
Fax: +44 (0) 141 429 2758

E-mail (Sales) [sales1@ftdichip.com](mailto:sales1@ftdichip.com)  
E-mail (Support) [support1@ftdichip.com](mailto:support1@ftdichip.com)  
E-mail (General Enquiries) [admin1@ftdichip.com](mailto:admin1@ftdichip.com)  
Web Site URL <http://www.ftdichip.com>  
Web Shop URL <http://www.ftdichip.com>

### Branch Office – Taipei, Taiwan

Future Technology Devices International Limited (Taiwan)  
2F, No 516, Sec. 1 NeiHu Road  
Taipei 114  
Taiwan, R.O.C.  
Tel: +886 (0) 2 8797 1330  
Fax: +886 (0) 2 8751 9737

E-mail (Sales) [tw.sales1@ftdichip.com](mailto:tw.sales1@ftdichip.com)  
E-mail (Support) [tw.support1@ftdichip.com](mailto:tw.support1@ftdichip.com)  
E-mail (General Enquiries) [tw.admin1@ftdichip.com](mailto:tw.admin1@ftdichip.com)  
Web Site URL <http://www.ftdichip.com>

### Branch Office – Hillsboro, Oregon, USA

Future Technology Devices International Limited (USA)  
7235 NW Evergreen Parkway, Suite 600  
Hillsboro, OR 97123-5803  
USA  
Tel: +1 (503) 547 0988  
Fax: +1 (503) 547 0987

E-Mail (Sales) [us.sales@ftdichip.com](mailto:us.sales@ftdichip.com)  
E-Mail (Support) [us.support@ftdichip.com](mailto:us.support@ftdichip.com)  
E-Mail (General Enquiries) [us.admin@ftdichip.com](mailto:us.admin@ftdichip.com)  
Web Site URL <http://www.ftdichip.com>

### Branch Office – Shanghai, China

Future Technology Devices International Limited (China)  
Room 408, 317 Xianxia Road,  
ChangNing District,  
ShangHai, China

Tel: +86 (21) 62351596  
Fax: +86(21) 62351595

E-Mail (Sales): [cn.sales@ftdichip.com](mailto:cn.sales@ftdichip.com)  
E-Mail (Support): [cn.support@ftdichip.com](mailto:cn.support@ftdichip.com)  
E-Mail (General Enquiries): [cn.admin1@ftdichip.com](mailto:cn.admin1@ftdichip.com)  
Web Site URL: <http://www.ftdichip.com>

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## Appendix C – Revision History

**Version 1.0** First Release

05/11/2010