TN_125 FT2232H Errata Technical Note

Document Reference No.: FT_000344

Version 1.0

Issue Date: 2010-11-05

The intention of this errata technical note is to give a detailed description of known functional or electrical issues with the FTDI FT2232H devices.
The current revision of the FT2232H is **revision C, released March 2010.**

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1 FT2232H Revision

FT2232H part numbers are listed in **Table 1.** The letter at the end of date code identifies the device revision.

The current revision of the FT2232H is **revision C, released March 2010.** At the time of releasing this Technical Note there are one known issues with this silicon revision. A workaround is provided for this issue.

Part Number	Package
FT2232HL	64 Pin LQFP
FT2232HQ	64 Pin QFN

Table 1 FT2232H Part Numbers

This errata technical note covers the revisions of FT2232H listed in **Table 2**.

Revision	Notes
A	First device revision
B	Second device revision
C	Third device revision

Table 2 FT2232H Revisions

2 Errata History Table – Functional Problems

Functional Problem	Short description	Errata occurs in device revision
FT2232H	Error reading EEPROM interface	A
FT2232H	Error reading internal FIFO in 245 Synchronous FIFO mode	A
FT2232H	3 Phase clocking in MPSSE mode incorrect	A
FT2232H	Wait on IO1 not functioning in CPU Emulation mode	A, B
FT2232H	Double bytes read in CPU Emulation mode	A, B, C

2.1 Errata History Table – Electrical and Timming Specification Deviations.

Deviations	Short description	Errata occurs in device revision
Suspend timer failure (USB Chapter 9 Compliance)	The USB specification requires a maximum time to suspend of 3.125ms. The device takes upto 4ms to suspend.	A, B

3 Functional Problems of FT2232H

3.1 Revision A

3.1.1 Error reading EEPROM Interface

Introduction:

The FT2232H uses an external EEPROM to store USB descriptors. These descriptors must be correctly read for the device to be properly identified and configured.

Problem:

There is an issue that under the right conditions the internal address counter can increment by 2 (incorrectly). This appears as though the data read from the EEPROM has missed a byte.

Workaround:

There are no known workarounds available. This issue is corrected at silicon revision B.

Package specific:

The effected packages are listed in Table 3.

Package	Applicable (Yes/No)
FT2232HL	Y
FT2232HQ	Y

Table 3

3.1.2 Error reading internal FIFO in 245 Synchronous FIFO mode

Introduction:

The FT2232H uses an internal FIFO to store received data from the synchronous FIFO interface. This FIFO is addressed one byte at a time.

Problem:

There is an issue that under the right conditions the internal address counter can increment by 2 (incorrectly). This appears as though the data read from the FIFO has missed a byte.

Workaround:

There are no known workarounds available. This issue is corrected at silicon revision B.

Package specific:

The effected packages are listed in Table 4.

Package	Applicable (Yes/No)
FT2232HL	Y
FT2232HQ	Y

Table 4

3.1.3 3 Phase clocking in MPSSE mode incorrect

Introduction:

The FT2232H introduced a new function to the MPSSE mode called 3 phase clocking to allow data to be clocked on both edges.

Problem:

3 Phase clocking was not being enabled.

Workaround:

There are no known workarounds available. This issue is corrected at silicon revision B.

Package specific:

The effected packages are listed in Table 5.

Package	Applicable (Yes/No)
FT2232HL	Y
FT2232HQ	Y

Table 5

3.2 Revision B

3.2.1 Wait on IO1 not functioning in CPU Emulation mode

Introduction:

The FT2232H has a "Wait On IO" feature in CPU mode to allow the processor to stop until the IO pin changes state.

Problem:

The Wait on IO is supposed to be routed to IO1. It is not.

Workaround:

There are no known workarounds available. This issue is corrected at silicon revision C.

Package specific:

The effected packages are listed in Table 3.

Package	Applicable (Yes/No)
FT2232HL	Y
FT2232HQ	Y

Table 6

3.3 Revision C

3.3.1 Double bytes read in CPU Emulation mode

Introduction:

The FT2232H has a CPU Emulation mode for transferring data.

Problem:

When reading a byte of data in CPU emulation mode the data is repeated. That is each byte of data is returned twice.

Workaround:

Switch off the divide by 5 clock divisor to resolve this problem (Command $8A)

Package specific:

The effected packages are listed in Table 7.

Package	Applicable (Yes/No)
FT2232HL	Y
FT2232HQ	Y

Table 7

4 Electrical and Timing specification deviations of FT2232H

4.1 Revision A

4.1.1 Suspend Timer Failure

Introduction:

The FT2232H has the ability to be put into suspend by the host to conserve power usage.

Problem:

The USB specification chapter 9 compliance tests require the device to go into suspend within 3.125ms. The device is taking upto 4ms to enter suspend state.

Workaround:

There are no known workarounds available. This issue is corrected at silicon revision C.

Package specific:

The effected packages are listed in Table 8.

Package	Applicable (Yes/No)
FT2232HL	Y
FT2232HQ	Y

Table 8

5   FT2232H Package Markings

FT2232H is available in a RoHS Compliant package, 64 pin LQFP and 64 pin QFN. An example of the markings on the package is shown in Figure 3-1.
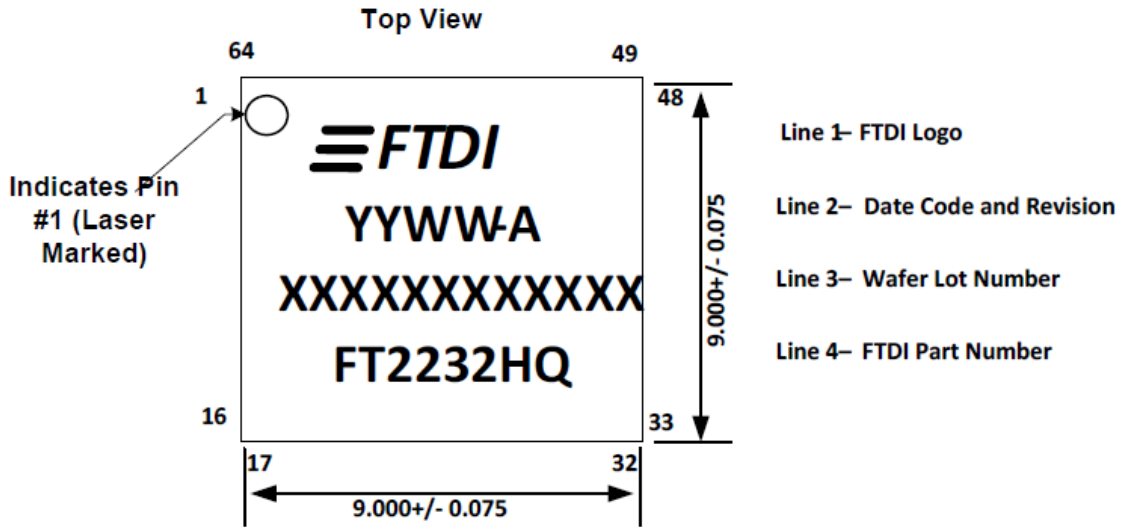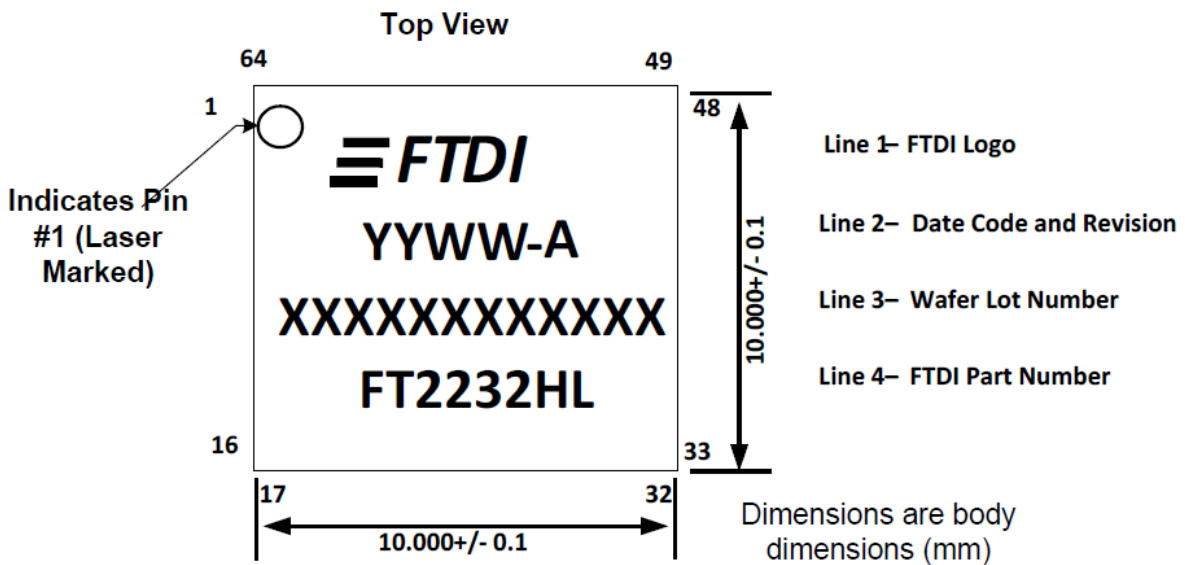

Figure 5-1 Package Markings – FT2232HQ

Figure 5-2 Package Markings – FT2232HL

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Appendix C – Revision History

Version 1.0 First Release   05/11/2010